REMARKS

As of the Office Action dated 9/23/2002, claims 1-29 and 50-53 were pending. Claims 1-19, 23-29, and 50-53 were rejected, while claims 20-22 were objected to. As of this response, claims 4, 8, 20, 22, 23, 25, and 27-29 are amended. Claims 17-19 are cancelled. New claims 54-115 are added. No new subject matter has been added. Claims 1-16, 20-29, and 50-115 are now pending. Reconsideration of the pending claims is requested in light of the following remarks.

Claim Rejections – 35 USC § 112

Claims 8 and 19 stand rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. In particular, the examiner requested explanation of the phrase "upper and lower portions of the package body with reference to the leads have different thickness each other." Claim 8 has been rewritten to provide additional clarity. Claim 19 has been cancelled. Applicants therefore respectfully submit that this rejection is overcome.

Claim Rejections – 35 USC § 102

Claims 1-3, 5, 8-10, and 50 stand rejected under 35 USC § 102(b) as being anticipated by U.S. Patent No. 5,014,113 issued to Casto ("Casto"). With regard to claims 1 and 50, Applicants respectfully disagree with the rejection for at least the following reasons:

Claims 1 and 50 require a chip attaching part 112b (see FIG. 3b) that has a thickness (t1) that is less than a thickness (t2) of the inner leads (116 of FIG. 3b). This limitation is not taught or disclosed by Casto. Nowhere does Casto reveal a thickness of the die bond flag 40 that is less than the thickness of the first frame layer 18. Casto appears only to support a teaching that the die bond flag 40 and first frame layer 18 are of the same thickness.

Furthermore, claim 50 also requires a package body of less than 0.7 mm of thickness. Casto discloses that the thickness of the first frame layer and second frame layer together are at least 5 mm thick (column 5, lines 24-27). Thus, the overall thickness of Casto's package body must be greater than 5 mm, and Casto fails to disclose the recited element of a package body of less than 0.7 mm.

The arguments presented above with respect to claim 1 also apply with respect to its dependent claims. In addition, claim 2 recites further details of the relationship between the chip attaching part and the lead thicknesses not disclosed by Casto. Casto is silent about the relative thicknesses of the two components, but states that when a die bond flag 40 is present, it is part of the first frame layer 18 (column 4, lines 30-32). This supports Applicants'

argument that the die bond flag 40 and the first frame layer 18 in Casto are of the same thickness. With respect to the figures, Casto explains that the proportions of the various parts are not drawn to scale, and that the thickness of various components in FIG. 1 are exaggerated for clarity (column 2, lines 54-57). It is therefore improper to infer anything about relative size from FIG. 1.

With respect to claim 5, Applicants' die pad (including the chip attaching part) and leads must be compared to Casto's die bond flag 40 and first frame layer 18, respectively. Claim 5 requires that the die pad is located below the lead frame. Casto, however, fails to teach or disclose any down-set between the die bond flag 40 and the horizontal top surface of the first frame layer 18.

Claim 8 requires different upper and lower thicknesses. Casto, however, appears only to teach embodiments in which the thickness of that package body above the leads 28 is equal to the thickness of that package body below the leads 18. For at least the foregoing reasons, Applicants respectfully submit that the 35 USC § 102 rejections to claims 1-3, 5, 8-10, and 50 are overcome.

Claim Rejections – 35 USC § 103

Claims 4, 6, 7, 12-14, and 51 were rejected under 35 USC § 103(a) as being unpatentable over Casto in view of U.S. Patent Application Publication 2002/0113305 by Huang ("Huang"). Applicants respectfully disagree for at least the following reasons:

Claims 4, 6, 7, and 12-14, are dependent upon claim 1. As noted previously, claim 1 requires that the thickness of the chip attaching part be less than the thickness of the inner leads. Neither Casto nor Huang disclose this limitation. A prima facie case of obviousness is therefore not established because the combination of Casto and Huang does not disclose all the limitations of claim 1.

Claim 51 depends from claim 50. As previously noted, Casto does not disclose different thicknesses for the chip attaching part and the inner lead, as required by claim 50. Huang also does not disclose this limitation. The combination of Casto and Huang therefore cannot form the basis for an obviousness rejection.

Claim 11 was rejected under 35 USC § 103(a) as being unpatentable over Casto in view of U.S. Patent No 5,818,105 issued to Kouda ("Kouda"). Claim 11 requires that the peripheral part protrude in both vertical directions from the chip attaching part, and that the thickness of the peripheral part is equal to the thickness of the leads. In Kouda (*see* FIG. 8), the peripheral part of die pad 89a only extends in one vertical direction (upwards) from the

chip attaching part, not both vertical directions. The combination of Casto and Kouda does not, therefore, supply all of the limitations of claim 11.

Claims 15 and 16 were rejected under 35 USC § 103(a) as being unpatentable over Casto in view of Huang and further in view of U.S. Patent No. 6,177,718 issued to Kozono ("Kozono"). Claims 15 and 16 depend from claim 1. As previously noted, neither Casto nor Huang disclose a chip attaching part having a thickness less than a thickness of inner leads. Kozono also fails to teach this limitation. The combination of Casto, Huang, and Kozono therefore fails to provide all of the limitations of claim 1 and its dependent claims 15 and 16.

Claims 17-19, 23-29, 52, and 53 were rejected under 35 USC § 103(a) as being unpatentable over Kouda in view of Huang. Claims 17-19 are cancelled. Claims 23, 25, and 27-29 are amended to depend from allowable claim 20. Claims 24 and 26 are dependent upon claims 23 and 25, respectively. All of these claims are therefore believed to be in condition for allowance.

Claim 52 requires a semiconductor package device having a package body of less than 0.7 mm of thickness. Kouda teaches that the package device in FIG. 8 can realize a package thickness of only 0.8 mm (column 8, lines 26-27). Huang also does not teach a semiconductor package device having a package body of less than 0.7 mm of thickness. A glance at Huang FIG. 1 reveals that Huang proposes a dual die pad structure (structures 410 and 440) that does not minimize package thickness. A prima facie case of obviousness has therefore not been established because the combination of Kouda and Huang does not teach or provide all of the limitations of claim 52. Claim 53 depends from claim 52 and is therefore also believed to be in condition for allowance.

For at least the reasons outlined above, the applicants submit that the 35 USC § 103 rejections to claims 4, 6, 7, 11-19, 23-29, and 51-53 are overcome, leaving those claims in condition for allowance.

Allowable Subject Matter

Claims 20-22 were indicated to be allowable over the prior art of record, if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claims 20 and 22 have been rewritten in independent form including all the limitations of base claim 17. Claim 21 has not been amended, since it already depends from allowable claim 20. The applicants submit that claims 20-22 are in condition for allowance.

New Claims

New claims 54-115 have been submitted. No new matter has been added. Claim 54

depends directly from claim 11 and indirectly from claim 1, and is therefore allowable for at least the reasons given with respect to claims 1 and 11, above.

Independent claim 55 requires that the thickness of the chip attaching part be less than the constant thickness of the inner leads. This limitation is absent in the prior art of record. Claim 55 further requires that the chip attaching part and the peripheral part have the same thickness. This limitation further distinguishes over Kouda. Claim 55 and its dependent claims are therefore believed to be patentable over the prior art of record.

Independent claim 71 requires that the chip attaching part have a first thickness and that a portion of the inner leads have a second thickness that is greater than the first thickness. It further requires that the bonding wires are connected to the portion of the inner leads, and that the chip attaching part and the peripheral part have the same thickness. These limitations distinguish over the prior art of record and claim 71 and its dependent claims are therefore believed to be in condition for allowance.

Independent claim 87 requires that the bonding wires connected to one of the first and the second semiconductor chips are shorter than the bonding wires connected to the other one of the first and the second semiconductor chips. This subject matter is found in the original application on page 4, lines 18-23, and in FIGS. 8 and 10, for example. These claims are also believed to be in condition for allowance.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1-16, 20-29, and 50-115 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

The claims have been amended as follows:

4. (Amended) An ultra-thin semiconductor package device according to claim 1 further comprising [two] another semiconductor [chips each attached to a corresponding side of the die pad chip attaching part] chip attached to a back side of the chip attaching part.

8. (Amended) An ultra-thin semiconductor package device according to claim 1, wherein an upper portion of the package body above the leads and a lower [portions] portion of the package body [with reference to the leads] below the leads have different [thickness each other] thicknesses.

Claims 17-19 are cancelled.

20. (Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and [An ultra-thin semiconductor package device according to claim 17,] wherein the peripheral part protrudes toward the second semiconductor chip.

22. (Amended) An ultra-thin semiconductor package device comprising:

a lead frame having a die pad, a plurality of leads disposed around the die pad, and a tie bar connected to the die pad, said die pad including a chip attaching part having a first thickness and a peripheral part surrounding and protruding away from the chip attaching part;

first and second semiconductor chips each including a plurality of electrode pads, wherein the first semiconductor chip is bonded to a top surface of the chip attaching part and the second semiconductor chip is bonded to a bottom surface of the chip attaching part;

a package body encapsulating the semiconductor chips; and

bonding wires configured to electrically connect the plurality of electrode pads and the leads, said leads having inner leads encapsulated with the package body to which the bonding wires are bonded and outer leads exposed from the package body, wherein the inner leads having a second thickness, wherein the first thickness is smaller than the second thickness, wherein the peripheral part has a thickness equal to the second thickness of the inner leads, and [An ultra-thin semiconductor package device according to claim 17,] wherein the bonding wires connected to one of the semiconductor chips are shorter than the bonding wires connected to the other semiconductor chip.

23. (Amended) An ultra-thin semiconductor package device according to claim [17] 20, wherein the bonding wires are connected by balls formed on the leads and stitches formed on the electrode pads.

25. (Amended) An ultra-thin semiconductor package device according to claim [17] 20, wherein the die pad comprises divided first and second die pads.

27. (Amended) An ultra-thin semiconductor package device according to claim [17] 20, wherein an adhesive bonds the semiconductor chip to the die pad chip attaching part.

28. (Amended) An ultra-thin semiconductor package device according to claim [17] 20, wherein a thickness of the package body is about 580 μm, a thickness of the die pad peripheral part is about 100 μm, and a thickness of the chip attaching part is about 40 μm.

29. (Amended) An ultra-thin semiconductor package device according to claim [17] 20, wherein an adhesive is attached to the backside of the chip in a wafer state to bond the semiconductor chips to the chip attaching part.

New claims 54-115 have been added.